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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/066,879 | 02/04/2002 | Dale E. Gulick | 2000.051700/TT4031 | 5870 |

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| EXAMINER | |
|---|---|
| DAMIANO, ANNE L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2114 | |

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/066,879 | GULICK, DALE E. | |
| | Examiner | Art Unit | |
| | Anne L Damiano | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statement filed 6/18/02 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

### *Specification*

2. The disclosure is objected to because of the following informalities: Page 30, lines 7, reference to "method 700 A" is believed be to a typographical error. The examiner believes this should read, "method 700 B".

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they

must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Claim 26 is followed by misnumbered claims 16-28. Then, following misnumbered claim 28, there is misnumbered claims 22-42

The following is the renumbering for the group of misnumbered claims following original, correctly numbered claim 26.

Misnumbered claims 16-28 have been renumbered to claims 27-39 respectively.

The following is the renumbering for the group of misnumbered claims following originally incorrectly numbered claim 28 (renumbered claims 39).

Misnumbered claims 22-42 have been renumbered to claims 40-60 respectively.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 40-60 are rejected under 35 U.S.C. 102(b) as being Poisner by (6,012,154).

As in claims 40, 47 and 54, Poisner discloses a method for operating an integrated circuit in a computer system, the method comprising:

entering a system state in the computer system (starting of the computer);

resetting a watchdog timer on the integrated circuit (column 2: lines 31-34);

determining an expiration of the watchdog timer on the integrated circuit (column 2: line 66-column 3: line 3);

evaluating the system state in the computer system (interrupt handler investigating malfunction); (column 3: lines 21-40) and

determining a system error in the computer system (column 5: lines 10-14); and

responding to the system error by a microcontroller on the integrated circuit (column 3: lines 21-40 and 5: lines 10-14). (The processor responds to a system error by running the Interrupt Handler.)

As in claims 41, 48 and 55, Poisner discloses the method of claims 40, 47 and 54, wherein resetting the watchdog timer on the integrated circuit comprises resetting the watchdog timer on the integrated circuit in response to entering the system state in the computer system (column 2: lines 31-34, and lines 43-44) (In response to entering the system state of the computer being on, the watchdog times is reset. However, also, when the timer expires and the system is in a state of malfunction and interrupt handler is called, the timer is also reset.)

As in claims 42, 49 and 56, Poisner discloses the method of claims 40, 47 and 54, wherein evaluating the system state in the computer system comprises evaluating the system state in the computer system in response to determining the expiration of the watchdog timer on

the integrated circuit (column 3: lines 21-40 and 5: lines 10-14). (When the timer expires, an interrupt is generated. When an interrupt causes the processor to execute the interrupt handler.)

As in claims 43, 50 and 57, Poisner discloses the method of claims 40, 47 and 54, further comprising: storing an indication of the system state (column 3: lines 56-62). (When a partial reset is called, due to the timer expiring, the system state information is retained.)

As in claims 44, 51 and 58, Poisner discloses the method of claims 43, 50 and 56, wherein storing the indication of the system state comprises storing the indication of the system state in a storage location on the integrated circuit (column 3: lines 62-67).

As in claims 45, 52 and 59, Poisner discloses the method of claims 43, 50 and 56, wherein storing the indication of the system state comprises storing the indication of the system state in response to entering the system state in the computer system (column 3: lines 56-67). (When the timer expires and a partial reset occurs, the indication of the system state is stored.)

As in claims 46, 53 and 60, Poisner discloses the method of claim 43, 50 and 56, wherein evaluating the system state in the computer system comprises reading the indication of the system state (column 3: lines 59-67). (When the computer is reset the indication of the system state is read.)

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-5, 9-18, 22-31 and 35-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Lindsay et al. (2003/0028633).

As in claims 1, 14 and 27, Lindsay discloses an integrated circuit, comprising:

a first bus interface logic (multi-protocol bus interface or NIC) for coupling to a first external bus;

a microcontroller configured as an Alert Standard Format management engine, wherein the microcontroller is further configured to receive Alert Standard Format sensor data over the first external bus (paragraphs 16, 37 and 115, figure 8: component 52); and

a watchdog timer coupled to the microcontroller, wherein the watchdog timer is coupled to receive a reset input upon a predetermined change in a system state, wherein the watchdog timer is further configured to provide an indication to the microcontroller in response to an expiration of the watchdog timer (paragraphs 51). (When it is determined that the primary power has changed the system state from not operating to operating, the watchdog timer is enabled and reset. If the watchdog timer expires, the ASF controller will be indicated.)

As in claims 2, 15 and 28, Lindsay discloses the integrated circuit of claims 1, 14 and 27, further comprising:

a second bus interface logic for coupling to a first internal bus (figure 8: SMBus and PCI bus), wherein data from the first

external bus is routable by the embedded Alert Standard Format management engine over the first internal bus (Paragraphs 16-18 and Figure 8).

As in claims 3, 16 and 29, Lindsay discloses the integrated circuit of claims 2, 15 and 28, further comprising:

an embedded Ethernet controller coupled to the first internal bus (paragraph 17).

As in claims 4, 17 and 30, Lindsay discloses the integrated circuit of claims 3, 16 and 29, wherein the embedded Ethernet controller is configured to route the Alert Standard Format sensor data from the embedded Alert Standard Format management engine to an external management server (paragraph 44).

As in claims 5, 18 and 31, Lindsay discloses the integrated circuit of claims 1, 14 and 27, wherein the indication provided to the microcontroller includes a microcontroller interrupt (PET) (paragraph.74, 75 and 115).

As in claims 9, 22 and 35, Lindsay discloses the integrated circuit of claim 1, 14 and 27, wherein the reset input is provided to the watchdog timer by the microcontroller (paragraph 113: lines 1-3).

As in claims 10, 23 and 36, Lindsay discloses the integrated circuit of claim 1, 14 and 27, wherein the reset input is provided to the watchdog timer from an external processor (paragraph 113: lines 3-6). (The NIC receives the start message from an external processor.)

As in claims 11, 24 and 37, Lindsay discloses the integrated circuit of claim 1, 14 and 27, the integrated circuit of claim 1, further comprising: a register configured to store system status information (paragraph 46).

As in claims 12, 25 and 38, Lindsay discloses the integrated circuit of claim 11, 24 and 37, wherein the microcontroller is further configured to read the system status information from the register in response to the indication (paragraph 46).

As in claims 13, 26 and 39, Lindsay discloses the integrated circuit of claim 12, 25 and 38, wherein the microcontroller is further configured to provide the system status information to an external management server (paragraph 74).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6-8, 19-21 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lindsay as applied to claims 1, 14 and 27 above and further in view of applicant's admitted prior art ("AAPA" hereafter).

Regarding claims 6, 19 and 32, Lindsay discloses the integrated circuit of claims 1, 14 and 27 above. However, Lindsay does not specifically disclose wherein the integrated circuit comprises a bridge.

AAPA discloses an integrated circuit comprising a bridge wherein the bridge further comprises: a third bus interface logic for coupling to a second external bus (Figure 1: components 114, 116, 112, 118, 115 and 110 and page 4: lines 1-8). (USB is an external bus)

It would have been obvious to a person skilled in the art at the time the invention was made to include a bridge with a third bus interface logic for coupling to a second external bus in the system taught by Lindsay. It would have been obvious because AAPA discloses an exemplary computer system including such. A person skilled in the art would have understood that chipsets typically use the Northbridge/Southbridge designations and that Lindsay's system was intended to include a bridge with a third bus interface logic for coupling to a second external bus.

As in claims 7, 20 and 33, AAPA discloses the integrated circuit of claims 6, 19 and 32, wherein the bridge comprises a south bridge, wherein the first external bus is configurable as a first input/output bus (figure 1A: component 115).

As in claims 8, 21 and 34, AAPA discloses the integrated circuit of claim 7, 20 and 33, wherein the first input/output bus is an SMBus (figure 1A: component 115).

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER